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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS

Appellants:	John Donohue
Serial No.	09/432,022
Filing Date	October 29, 1999
Group Art Unit	2631
Examiner	Pankaj Kumar
Attorney Docket No.	100.003US01

APPEAL BRIEF

Title: SYSTEMS AND METHODS FOR HOLDOVER CIRCUITS IN PHASE LOCKED LOOPS

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1. Real Party in Interest

The real party in interest in the above-captioned application is the assignee ADC Telecommunications, Inc.

2. Related Appeals and Interferences

There are no other appeals or interferences known to Appellant which will have a bearing on the Board's decision in the present appeal.

3. Status of the Claims

Claims 1-31 are pending in the application.

Claims 15-22 are allowed.

Claims 4-7, 9 and 13 are objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1, 2, 3, 8, 10-12, 14, and 23-31 are rejected.

Claims 23-31 stand rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention.

Claims 1, 2, 3, 8, 10, 14, 23, 24, 26, and 30 stand rejected under 35 USC § 102(b) as being anticipated by Abe et al. (U.S. Patent No. 5,319,320) (also referred to here as "Abe").

Claims 11, 12, 27, and 28 stand rejected under 35 USC § 103(a) as being unpatentable over Abe et al. (U.S. Patent No. 5,319,320) in view of Satoshi (JP 56051140) (also referred to here as "Satoshi").

Claim 31 stands rejected under 35 USC § 103(a) as being unpatentable over Abe et al. (U.S. Patent No. 5,319,320).

4. Status of Amendments

In Appellant's Amendment After Final filed on August 18, 2003, an amendment to claim 25 was proposed to address a typographical error. The proposed amendment was entered in the Advisory Action, mailed on August 28, 2003.

5. Summary of the Invention

The present invention is directed to an improved phase locked loops that includes the capability to "hold" the output clock in a communication system at or very near the last output frequency before the loss of input data. This can prevent loss of data and communication with successive locations, or minimize disruption in communication, by avoiding rapid changes in data transmission rates.

In particular, an illustrative embodiment of the present invention (shown in FIG. 2 and described on page 4, line 24 – page 6, line 30 of the specification) includes a phase locked loop (200) which "holds" the output clock in a communication system at or very near the last output frequency before the loss of input data. The phase locked loop according to the teachings of the present invention includes a differential phase detector (202) that receives an input signal (204) and a feedback signal (206) and produces a differential output signal (208). An electronic selector circuit (210) is coupled to a differential output of the phase detector with an input that is responsive to a detected state of the input signal.

An operational amplifier based loop filter circuit (212) is provided in the phased locked loop. The electronic selector circuit provides the differential output of the phase detector at a pair of inputs (218A and 218B) to the operational amplifier. A voltage controlled oscillator (226) is coupled to an output of the operational amplifier and provides an output frequency (228) for the phased locked loop circuit. The electronic selector circuit is operable to control the input to the operational amplifier to hold an output frequency of the voltage controlled oscillator at a substantially constant frequency.

In the embodiment shown in FIG. 2, the electronic selector circuit includes a switch (220) which couples the pair of inputs together when a reference signal, or input signal to the phase detector is interrupted. In another embodiment (shown in FIG. 3 and described on page 7, line 1 – page 9, line 29), the electronic selector circuit includes a logic-based selector circuit (310) which holds the pair of inputs (318A and 318B) to an identical potential level when the input signal (304) to the phase detector (302) is interrupted.

6. Issues Presented for Review

The first question presented in this Appeal is whether the Examiner erred in rejecting claims 23-31 under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention.

The second question presented in this Appeal is whether the Examiner erred in rejecting claims 1, 2, 3, 8, 10, 14, 23, 24, 26, and 30 under 35 USC § 102(b) as being anticipated by Abe et al. (U.S. Patent No. 5,319,320).

The third question presented in this Appeal is whether the Examiner erred in rejecting claims 11, 12, 27, and 28 under 35 USC § 103(a) as being unpatentable over Abe et al. (U.S. Patent No. 5,319,320) in view of Satoshi (JP 56051140).

The fourth question presented in this Appeal is whether the Examiner erred in rejecting claim 31 under 35 USC § 103(a) as being unpatentable over Abe et al. (U.S. Patent No. 5,319,320).

7. Grouping of Claims

Each of claims 1-3, 7-14, and 23-31 stands or falls on its own merits

8. Argument

A. Rejection of Claims 23-31 under 35 U.S.C. § 112, Second Paragraph

1. Applicable Law

35 U.S.C. § 112, second paragraph, states:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Under Section 112, claims must be particular and distinct. The primary purpose of this requirement of definiteness in claims is to provide clear warning to others as to what constitutes infringement of the patent. *See, e.g., Solomon v. Kimberly-Clark Corp.,* 216 F.3d 1372, 55 USPQ2d 1279 (Fed. Cir. 2000). A secondary purpose is to provide a clear measure of the invention in order to facilitate determinations of patentability. *See, e.g., In re Hammack,* 427 F.2d 1378, 1382, 166 USPQ 204 (CCPA 1970).

2. Analysis

In the Final Office Action (mailed June 18, 2003), the Examiner took the position that claim 23 was rejected because "'the input signal' does not specify first, second or some other input signal." *See* Final Office Action, page 4, paragraph 7. The Examiner rejected claims 24-31 since those claims depended from claim 23. *See* Final Office Action, page 4, paragraph 9.

In the Advisory Action, the Examiner maintained the rejection of claims 23-31 under 35 USC § 112, second paragraph "since there is confusion as to the relationship between 'input data' and 'input signal.'" *See* Advisory Action, page 2, paragraph 3.

Claim 23 of the present application is directed to a "method for preventing data errors in a communication system, comprising: coupling *input data* to *a phase locked loop circuit.*" Claim 23 further recites "wherein the phase locked loop includes: *a differential phase detector* that receives *an input signal* and a feedback signal and produces a differential output signal."

The Examiner has failed to make out a *prima facie* case of indefiniteness under 35 USC § 112, second paragraph. The Examiner provides no explanation as to why the Examiner believes

there is confusion between the relationship between "input data" and "input signal." That both phrases include the word "input" is not confusing since one of ordinary skill in the art is able to distinguish between "input data" coupled to a *phase locked circuit* and an input signal received at *a differential phase detector*. Moreover, the Examiner has failed to provide any basis for why a relationship must be specified in claim 23 between the "input data" and the "input signal."

Claims 24-31 were rejected under 35 USC § 112, second paragraph, because these claims depended from claim 23. Therefore, the Examiner erred in rejecting claims 24-31 for the reasons set forth above with respect to claim 23.

B. Rejection of Claims 1-3, 8, 10, 14, 23, 24, 26, and 30 under 35 USC § 102(b)

1. Applicable Law

35 U.S.C.§ 102 provides in relevant part:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in a public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A claim is anticipated under 35 U.S.C.§ 102 only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but identical terminology is not required. *In re Bond,* 910 F. 2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990).

Anticipation focuses on whether a claim reads on a product or process disclosed in a prior art reference, not on what the reference broadly teaches. *Kalman v. Kimberyl-Clark Corp.,* 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). To anticipate a claim, a reference must disclose every element of the challenged claim and enable one skilled in the art to make the anticipating subject matter. *PPG Industries, Inc. v. Guardian Industries Corp.,* 75 F.3d 1558, 37 U.S.P.Q.2d

1618 (Fed. Cir. 1996).

2. Analysis

Claim 1 of the present application is directed to a "phase locked loop circuit" that recites, in relevant part, "a differential phase detector that receives *an input signal* and *a feedback signal* and produces a differential output signal" and "wherein the electronic selector circuit is operable to control the amplifier input *to hold the output frequency of the voltage controlled oscillator* at a substantially constant frequency *when the input signal to the phase detector is interrupted.*"

The Examiner erred in rejecting claim 1 under 35 USC § 102(b). In particular, Abe does not teach "wherein the electronic selector circuit is operable to control the amplifier input to hold the output frequency of the voltage controlled oscillator at a substantially constant frequency when the input signal to the phase detector is interrupted" as recited in claim 1.

The Examiner took the position that the interruption of the VCO (item 50 in FIG. 1 and item 40 in FIG. 4) of Abe causes an interruption of at least one input of the phase comparator (item 60 in FIG. 1 and item 10 in FIG. 4) of Abe. The Examiner, in the Final Office Action, cited paragraphs 5 and 6 of Abe in rejecting claim 1 of the present application. The following portion of paragraphs 5 and 6 of Abe are cited in the Final Office Action:

> Since oscillation frequency f.sub.OSC of voltage-controlled oscillator 40 is varied by the value of the filter output voltage V.sub.F, the phase difference between oscillator output V.sub.OUT and input signal S.sub.IN becomes zero as time progresses.
>
> During a time in which signals X.sub.1, X.sub.2 of each period are not generated, an integrated load is stored in capacitor C.sub.F, and, therefore, the output of voltage-controlled oscillator 40 is controlled by that charging voltage. Therefore, the charging voltage of capacitor C.sub.F for current i functions as a frequency control signal for the pull-in operation that matches oscillation frequency f.sub.OSC to the frequency of input signal S.sub.IN.

Abe, column 1, line 57 – column 2, line 1. The Final Office Action then goes on to reason that "when the output of VCO is 0, at least one input of the phase comparator, element 60 in fig 1, is

interrupted." Thus, the Examiner is taking the position that it is the output of the VCO (item 50 in FIG. 1 and item 40 in FIG. 4 of Abe) that is interrupted and that the interruption of the output of the VCO causes interruption of at least one input of the phase comparator (item 60 in FIG. 1 and item 10 in FIG. 4 of Abe). *See also,* Advisory Action, page 2, paragraph 4.

The output of the VCO of Abe cannot properly be considered an "input signal" in the context of claim 1 of the present application. Claim 1 of the present application recites "a differential phase detector that receives *an input signal* and *a feedback signal.*" In other words, in the context of claim 1 of the present application, there is a distinction between "the input signal" received by the differential phase detector and "the feedback signal" received by the differential phase detector. The output of the VCO 50 of Abe is a "feedback signal" received by the phase comparator 60 of Abe. It is not an "input signal" as that term is used in the context of claim 1 of the present application. In fact, this same distinction is made in Abe: "A phase-locked loop 100 comprises a digital phase comparator (PC) 60 which compares the phase of an *input signal* S_{IN}, as a reference signal, with the phase of an *output* V_{OUT} (at oscillation frequency f_{OSC}) of *a voltage-controlled oscillator 50. . . .*" Abe, column 5, line 66 – column 6, line 3. See also, for example, claim 1 of Abe ("A phase-locked loop that detects the phase difference between *an input signal*, which is a reference signal, and *an oscillator output.*"). Therefore, regardless of whether or not the output of VCO 50 is interrupted, the output of VCO 50 cannot properly be considered "an input signal" (as opposed to "a feedback signal") as recited in claim 1 of the present application. Accordingly, Abe does not teach or suggest "wherein the electronic selector circuit is operable to control the amplifier input to hold the output frequency of the voltage controlled oscillator at a substantially constant frequency *when the input signal to the phase detector is interrupted.*"

In the Advisory Action, the Examiner responded to this argument as follows:

> This argument is not persuasive since, as Abe discusses, the difference between the input signal and feedback signal becomes 0 as time progresses. Thus, in Abe, the value of the input signal and the feedback signal is the same as time progresses. Accordingly, as time progresses, if the feedback signal is interrupted, the input signal is also interrupted.

Advisory Action, page 2, paragraph 6. In other words, the Examiner is arguing that the feedback signal somehow affects the input signal so that if the feedback signal is interrupted, the input signal is interrupted.

The proposition that the feedback signal (that is, the output of the VCO 40, 50) somehow affects the input signal (that is, SIN) is wholly without support in Abe. The Examiner provides no citation to any part of Abe that supports this. That the difference between some aspect (phase) of the feedback signal and the input signal goes to zero *is due to the feedback function provided by the circuit of Abe.* Abe in no way teaches that the feedback signal is somehow used to control or otherwise affect the input signal SIN—the input signal is a *separate input* to the phase comparator 10, 60.

Furthermore, Abe does not teach that the feedback signal (that is, the output of the VCO 40, 50) of Abe is interrupted. The portion of Abe cited in the Final Office Action (paragraphs 5 and 6 of Abe) indicates that the phase difference *between* the input signal SIN *and* the feedback signal VCO becomes zero as time progresses due to the feedback function provided by the Abe circuit. In other words, the output of the phase comparator 10, 60 becomes zero, not the output of VCO 40, 50. This does not support the proposition that the feedback signal VCO is interrupted. Nothing in FIGS. 3 or 6 of Abe shows the feedback signal being interrupted.

In addition, it is respectfully submitted that nowhere does the Examiner explain how the output frequency of the voltage controlled oscillator is held at a substantially constant frequency when the input signal to the phase detector is interrupted, as recited in claim 1 of the present application. It is respectfully submitted that the Examiner's arguments are internally inconsistent on this point. The Examiner has not explained how the output of the VCO 40, 50 of Abe is held at a substantially constant frequency while at the same being interrupted.

Accordingly, it is respectfully submitted that the Examiner erred in rejecting claim 1 of the present application under 35 USC § 102(b).

Claims 2 and 3 depend from claim 1 and therefore the arguments set forth above with respect to claim 1 also apply to theses claims.

Claim 2 of the present application further recites "wherein the electronic selector circuit de-couples the amplifier input from the differential output *and* holds the output frequency under an external command *when the input signal to the phase detector is interrupted.*" Claim 3 depends from claim 2 and further recites "wherein the electronic selector circuit holds a current signal input to the operational amplifier when a reference signal to the phase detector is interrupted."

The Examiner erred in rejecting claims 2 and 3 under 35 USC § 102(b) since the additional features recited in these claims are not taught in Abe. In the Final Office Action, the Examiner argued with respect to claim 2 that "if X1 is high and X2 is low then V1 will not change as shown in fig. 3 and thus 60, in fig. 1 is decoupled." Final Office Action, page 6, paragraph 14. However, the Examiner does not explain how this occurs when the input signal to the phase detector is interrupted.

In the Advisory Action, in connection with a similar argument made with respect to claim 8, the Examiner took the position that the phrase "when the input signal to the phase detector is interrupted" does not modify the phrase "de-couples the amplifier input from the differential output." Advisory Action, page 3, paragraph 1. Applicant respectfully submits that this interpretation is incorrect. Claim 2 reads "wherein the electronic selector circuit de-couples the amplifier input from the differential output *and* holds the output frequency under an external command *when the input signal to the phase detector is interrupted.*" There is no punctuation or other grammatical feature that indicates that the phrase "when the input signal to the phase detector is interrupted" does not modify the phrase "de-couples the amplifier input from the differential output."

Accordingly, it is respectfully submitted that the Examiner erred in rejecting claims 2 and 3 of the present application under 35 USC § 102(b).

Claim 8 of the present application is directed to a phase locked loop circuit. In relevant

part, claim 8 recites "a differential phase detector that receives an input signal and a feedback signal and produces a differential output signal" and "wherein the electronic selector circuit de-couples the amplifier input from the differential output *and* holds the output frequency of the voltage controlled oscillator to a last received signal from the differential output *when the input signal to the phase detector is interrupted.*"

The Examiner erred in rejecting claim 8 since Abe fails to teach "wherein the electronic selector circuit de-couples the amplifier input from the differential output *and* holds the output frequency of the voltage controlled oscillator to a last received signal from the differential output *when the input signal to the phase detector is interrupted.*" For the same reasons set forth above respect to claim 1, the Examiner erred in rejecting claim 8 of the present application under 35 USC § 102(b) since Abe fails to teach any operation occurring when an "input signal to the phase detector is interrupted."

Moreover, the Examiner failed to show how Abe teaches such de-coupling when the input signal to the phase detector is interrupted. Instead as noted above, in the Advisory Action the Examiner took the position that the phrase "when the input signal to the phase detector is interrupted" does not modify the phrase "de-couples the amplifier input from the differential output." Advisory Action, page 3, paragraph 1. For reasons set forth above in connection with claim 2 and 3, this interpretation is incorrect.

Accordingly, it is respectfully submitted that the Examiner erred in rejecting claim 8 of the present application under 35 USC § 102(b).

Claims 10 and 14 of the present application depend from claim 8. Therefore, based on the arguments set forth above with respect to claim 8, it is respectfully submitted that the Examiner erred in rejecting claims 10 and 14 of the present application.

Moreover, claims 10 and 14 recite additional features that are not taught by Abe. For example, claim 10 further recites "wherein the amplifier input includes a pair of amplifier inputs and wherein the electronic selector circuit includes a logic-based selector circuit which holds the pair of amplifier inputs to an identical potential level to hold the last received signal from the

differential output at the operational amplifier when the input signal to the phase detector is interrupted." In the Final Office Action, the Examiner took the position that V2 shown in FIG. 3 is constant at some places. Final Office Action, page 7, paragraph 17. However, no explanation is provided as to how this occurs when the input signal to the phase detector is interrupted.

Accordingly, it is respectfully submitted that the Examiner erred in rejecting claims 10 and 14 of the present application under 35 USC § 102(b).

Claim 23 of the present application is directed to a method for preventing data errors in a communication system. Claim 23 recites, in relevant part, "wherein the phase locked loop includes: a differential phase detector that receives an input signal and a feedback signal and produces a differential output signal" and "using the electronic selector circuit to control the amplifier input to hold the output frequency of the voltage controlled oscillator at a substantially constant frequency when the input signal to the phase detector is interrupted."

Claims 24, 26, and 30 of the present application depend from claim 23.

The Examiner claims 23, 24, 26, and 30 for the same reasons set forth above with respect to the other claims. Therefore, based on the arguments set forth above, the Examiner erred in rejecting claims 23, 24, 26, and 30 under 35 USC § 102(b).

C. Rejection of Claims 11, 12, 27, and 28 under 35 USC § 103(a)

1. Applicable Law

35 U.S.C.§ 103 provides in relevant part:

Conditions for patentability; non-obvious subject matter.

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

"The ultimate determination . . . whether an invention is or is not obvious is a legal conclusion based on underlying factual inquiries including: (1) the scope and content of the prior art; (2) the level of ordinary skill in the prior art; (3) the differences between the claimed invention and the prior art; and (4) objective evidence of nonobviousness." *In re Dembiczak*, 175 F.3d 994, 998, 50 USPQ2d 1614, 1616 (1999) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966)).

When applying 35 U.S.C. §103, the claimed invention must be considered as a whole; the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention and a reasonable expectation of success is the standard with which obviousness is determined. *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2143

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. MPEP 2143 citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

2. Analysis

Claim 11 of the present application ultimately depends from claim 8 and therefore the arguments set forth above with respect to claim 8 apply to claim 11 as well. Furthermore, claim 11 further recites "wherein the logic based selector circuit includes a pair of AND gates, each AND gate having an output coupled to one of the pair of amplifier inputs, wherein one input of each AND gate is coupled to the differential output, and wherein the other input of each AND

gate is coupled to an external command signal source."

In the Final Office Action, the Examiner conceded that Abe does not disclose the features recited in claim 11 of the present application. The Examiner then asserted that Satoshi teaches the features recited in claim 11—referring to AND gates 81, 82 of Satoshi. The Examiner asserted that it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Abe to includes the AND gates in Satoshi as claimed in claim 11. The Examiner concluded that "One would be motivated to do so for the purpose stated in its [Satoshi's] abstract." Final Office Action, page 10, paragraph 25.

> The stated "PURPOSE" set forth in the Abstract of Satoshi is as follows:
>
> To prevent the lock failure, by detecting whether the amplitude of the AM-modulated carrier is a fixed value or more or not and by stopping the phase comparison function if it is a fixed value or less, in respect to the PLL of the AM stereo receiver.

The Examiner provides no explanation whatsoever as to how this stated purpose, which relates to an AM stereo receiver, is at all relevant to a circuit used with hard disk drives (Abe, column 1, lines 6-10). Applicant respectfully submits that the Examiner is using impermissible hindsight in making this proposed modification.

Moreover, Satoshi does not teach "each AND gate having an output coupled to one of the pair of amplifier inputs" as recited in claim 11 of the present application. Satoshi does not mention amplifier inputs at all (*See, for example,* Satoshi, Figure, output of AND gate 81, 82 coupled to charge pump 50).

Accordingly, it is respectfully submitted that the Examiner erred in rejecting claim 11 of the present application under 35 USC § 103(a).

Claim 12 depends from claim 11 (which ultimately depends from claim 8). Therefore, the arguments set forth above with respect to claim 8 above apply to claim 12 as well. Moreover, claim 12 further recites "wherein the external command signal source provides a high potential to one input of each AND gate."

In the Final Office Action, the only support provided for the rejection of claim 12 is the statement "Satoshi figure." The Examiner provides no explanation as to how Satoshi teaches the recited feature, nor why one of ordinary skill in the art would be motivated to make the proposed modification. Thus, a *prima facie* case of obviousness has not been made out. Moreover, the same arguments made above with respect to claim 11 apply to claim 12 as well.

Accordingly, it is respectfully submitted that the Examiner erred in rejecting claim 12 of the present application under 35 USC § 103(a).

Claim 27 ultimately depends from claim 24 and therefore the arguments set forth above with respect to claim 24 apply to claim 27 as well. Moreover, claim 27 further recites "wherein using a logic-based selector circuit to hold the pair of amplifier inputs to an identical potential level includes using a logic-based selector circuit having a pair of AND gates, coupling an output of each AND gate to one of the pair of amplifier inputs, coupling one input of each AND gate to the differential output, and coupling the other input of each AND gate to an external command signal source."

Claim 28 depends from claim 27 (which ultimately depends from claim 24). Therefore, the arguments set forth above with respect to claim 24 apply to claim 28 as well. Furthermore, claim 28 further recites "wherein using a logic-based selector having a pair of AND gates and coupling the other input of each AND gate to an external command signal source includes coupling the other input of each AND gate to a high potential."

The Examiner rejected claims 27 and 28 for apparently the same reasons as claims 11 and 12. Therefore, Applicant respectfully submits that the Examiner erred in rejecting claims 27 and 28 under section 103(a) for the same additional reasons set forth above with respect to claims 11 and 12, respectively.

D. Rejection of Claim 31 under 35 USC § 103(a)

1. Applicable Law

See section 8.C.1.

2. Analysis

Claim 31 depends from claim 23 and, therefore, the arguments set forth above with respect to claim 23 apply to claim 31 as well. Moreover, claim 31 further recites "wherein the method further includes using the output frequency of the voltage controlled oscillator as an output frequency for a system clock coupled to a number of system modules connected to the communication system."

In the Final Office Action, the Examiner took the position that "It would have been obvious to one skilled in the art at the time of the invention to modify Abe to teach system clock and communication system since it has been held that the selection of known material (in this case, system clock or communication system) based on its suitability for the intended use for prior art parts does not make the claimed invention patentable over the prior art (In re Leshin, 125 USPQ 416). Also, applicant appears to compare [sic?] the method or manner of intended use of the apparatus rather to delineating claimed structure not shown or made obvious by the prior art." Final Office Action, page 11, paragraph 30.

The Examiner erred in rejecting claim 31 of the present application. As an initial matter, claim 31 is directed to a *method.* The recitation of "using the output frequency of the voltage controlled oscillator as an output frequency for a system clock coupled to a number of system modules connected to the communication system" is not a recitation of an intended use in an apparatus claim, but instead is the recitation of a specific feature of a method.

Moreover, the Examiner has failed to provide any motivation whatsoever to make the proposed modification.

Accordingly, it is respectfully submitted that the Examiner erred in rejecting claim 31 of the present application under 35 USC § 103(a).

9. Conclusion

Appellant has set forth reasons why the Examiner is incorrect in maintaining the rejections of the pending claims. Specifically, the Examiner has failed to set forth a *prima facie* case of indefiniteness under 35 U.S.C. §112, second paragraph, a *prima facie* case of anticipation

under 35 U.S.C. §102(b), and a *prima facie* case of obviousness under 35 U.S.C. §103(a). None of the references cited alone or in combination teach or suggest all the elements in the pending independent and dependant claims. Therefore, reversal of the Examiner's rejections is respectfully requested.

Respectfully submitted,

Date: 11/24/2003

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Appendix 1

The Claims on Appeal

1. A phase locked loop circuit, comprising:

a differential phase detector that receives an input signal and a feedback signal and produces a differential output signal;

an electronic selector circuit having:

at least one first input coupled to the differential output signal of the phase detector; and

a second input that is responsive to a detected state of the input signal;

a loop filter circuit having an operational amplifier, the operational amplifier having at least one amplifier input, wherein the electronic selector circuit provides the differential output signal of the phase detector to the amplifier input;

a voltage controlled oscillator coupled to an output of the operational amplifier and providing an output frequency for the phased locked loop circuit; and

wherein the electronic selector circuit is operable to control the amplifier input to hold the output frequency of the voltage controlled oscillator at a substantially constant frequency when the input signal to the phase detector is interrupted.

2. The circuit of claim 1, wherein the electronic selector circuit de-couples the amplifier input from the differential output and holds the output frequency under an external command when the input signal to the phase detector is interrupted.

3. The circuit of claim 2, wherein the electronic selector circuit holds a current signal input to the operational amplifier when a reference signal to the phase detector is interrupted.

4. The circuit of claim 3, wherein the amplifier input includes a pair of amplifier inputs and wherein the electronic selector circuit holds a current signal input to the operational amplifier by coupling the pair of amplifier inputs at the same potential.

5. The circuit of claim 4, wherein the electronic selector circuit includes a switch which couples the pair of amplifier inputs together when the reference signal to the phase detector is interrupted.

6. The circuit of claim 2, wherein the amplifier input includes a pair of amplifier inputs and wherein the electronic selector circuit includes a logic-based selector circuit which holds the pair of amplifier inputs to an identical potential level when the input signal to the phase detector is interrupted.

7. The circuit of claim 2, wherein the electronic selector circuit re-couples the amplifier input to the differential output of the phase detector when the input signal is restored.

8. A phase locked loop circuit, comprising:

a differential phase detector that receives an input signal and a feedback signal and produces a differential output signal;

an electronic selector circuit having:

at least one first input coupled to the differential output signal of the phase detector; and

a second input that is responsive to a detected state of the input signal;

a loop filter circuit having an operational amplifier, the operational amplifier having at least one amplifier input, wherein the electronic selector circuit provides the differential output signal of the phase detector to the amplifier input;

a voltage controlled oscillator coupled to an output of the operational amplifier and providing an output frequency for the phased locked loop circuit; and

wherein the electronic selector circuit de-couples the amplifier input from the differential output and holds the output frequency of the voltage controlled oscillator to a last received signal from the differential output when the input signal to the phase detector is interrupted.

9. The circuit of claim 8, wherein the amplifier input includes a pair of amplifier inputs and wherein the electronic selector circuit includes a switch which couples the pair of amplifier inputs together to hold the last received signal as a current signal input to the operational amplifier when the input signal is interrupted.

10. The circuit of claim 8, wherein the amplifier input includes a pair of amplifier inputs and wherein the electronic selector circuit includes a logic-based selector circuit which holds the pair of amplifier inputs to an identical potential level to hold the last received signal from the differential output at the operational amplifier when the input signal to the phase detector is interrupted.

11. The circuit of claim 10, wherein the logic based selector circuit includes a pair of AND gates, each AND gate having an output coupled to one of the pair of amplifier inputs, wherein one input of each AND gate is coupled to the differential output, and wherein the other input of each AND gate is coupled to an external command signal source.

12. The circuit of claim 11, wherein the external command signal source provides a high potential to one input of each AND gate.

13. The circuit of claim 8, wherein the electronic selector circuit re-couples the amplifier input to the differential output of the phase detector when the input signal to the phase detector is restored.

14. The circuit of claim 8, wherein the output frequency of the voltage controlled oscillator provides the feedback signal to the differential phase detector.

15. A communication system, comprising:

a number of traffic cards having traffic inputs and traffic outputs;

a switching device coupled to the number of traffic cards; and

a synchronization source, coupled to the number of traffic cards, having a selector coupled to an external synchronization source and a controller, wherein the selector provides an input signal to a phased locked loop circuit, wherein the phase locked loop circuit is coupled to the controller, and wherein the phase locked loop circuit includes:

a differential phase detector that receives the input signal and a feedback signal and produces a differential output signal;

an electronic selector circuit having:

at least one first input coupled to the differential output signal of the phase detector; and

a second input that is responsive to a detected state of the input signal;

a loop filter circuit having an operational amplifier, the operational amplifier having at least one amplifier input, wherein the electronic selector circuit provides the differential output signal of the phase detector to the amplifier input;

a voltage controlled oscillator coupled to an output of the operational amplifier and providing an output frequency for the phased locked loop circuit; and

wherein the electronic selector circuit de-couples the amplifier input from the differential output and holds the output frequency of the voltage controlled oscillator to a last received signal from the differential output when the input signal to the phase detector is interrupted.

16. The system of claim 15, wherein the amplifier input includes a pair of amplifier inputs and wherein the electronic selector circuit includes a switch which couples the pair of amplifier inputs together to hold the last received signal as a current signal input to the operational amplifier under an instruction from the controller when the input signal is interrupted.

17. The system of claim 15, wherein the amplifier input includes a pair of amplifier inputs and wherein the electronic selector circuit includes a logic-based selector circuit which holds the

pair of amplifier inputs to an identical potential level, under an instruction from the controller, to hold the last received signal from the differential output at the operational amplifier when the input signal to the phase detector is interrupted.

18. The system of claim 17, wherein the logic based selector circuit includes a pair of AND gates, each AND gate having an output coupled to one of the pair of amplifier inputs, wherein one input of each AND gate is coupled to the differential output, and wherein the other input of each AND gate is coupled to an external command signal from the controller.

19. The system of claim 18, wherein the external command signal includes a high potential signal provided to one input of each AND gate.

20. The system of claim 15, wherein the electronic selector circuit re-couples the amplifier input to the differential output of the phase detector when the input signal is restored.

21. The system of claim 15, wherein the output frequency of the voltage controlled oscillator provides the feedback signal for the differential phase detector.

22. The system of claim 15, wherein the output frequency of the voltage-controlled oscillator further serves as a system clock to a number of system modules connected to the communication system.

23. A method for preventing data errors in a communication system, comprising:

coupling input data to a phase locked loop circuit, wherein the phase locked loop includes:

a differential phase detector that receives an input signal and a feedback signal and produces a differential output signal;

an electronic selector circuit having:

at least one first input coupled to the differential output signal of the phase detector; and

a second input that is responsive to a detected state of the input signal;

a loop filter circuit having an operational amplifier, the operational amplifier having at least one amplifier input, wherein the electronic selector circuit provides the differential output signal of the phase detector to the amplifier input; and

a voltage controlled oscillator coupled to an output of the operational amplifier and providing an output frequency for the phased locked loop circuit;

using the electronic selector circuit to control the amplifier input to to hold the output frequency of the voltage controlled oscillator at a substantially constant frequency when the input signal to the phase detector is interrupted; and

using the electronic selector circuit to release control of the amplifier input to follow the differential output when the input signal to the phase detector is restored.

24. The method of claim 23, wherein the amplifier input includes a pair of amplifier inputs and wherein using the electronic selector circuit to hold the output frequency of the voltage controlled oscillator at a substantially constant frequency includes using the electronic selector circuit to de-couple the pair of amplifier inputs from the differential output and hold the output frequency of the voltage controlled oscillator to a last received signal from the differential output when the input signal to the phase detector is interrupted.

25. The method of claim 24, wherein using the electronic selector circuit to de-couple the pair of amplifier inputs from the differential output includes using a switch to couple the pair of amplifier inputs together to hold the last received signal as a current signal input to the operational amplifier when the input signal is interrupted.

26. The method of claim 24, wherein using the electronic selector circuit to de-couple the

pair of amplifier inputs from the differential output includes using a logic-based selector circuit to hold the pair of amplifier inputs to an identical potential level in order to hold the last received signal from the differential output at the operational amplifier when the input signal to the phase detector is interrupted.

27. The method of claim 26, wherein using a logic-based selector circuit to hold the pair of amplifier inputs to an identical potential level includes using a logic-based selector circuit having a pair of AND gates, coupling an output of each AND gate to one of the pair of amplifier inputs, coupling one input of each AND gate to the differential output, and coupling the other input of each AND gate to an external command signal source.

28. The method of claim 27, wherein using a logic-based selector having a pair of AND gates and coupling the other input of each AND gate to an external command signal source includes coupling the other input of each AND gate to a high potential.

29. The method of claim 23, wherein the amplifier input includes a pair of amplifier inputs and wherein using the electronic selector circuit to release control of the amplifier input to follow the differential output includes using the electronic selector circuit to re-couple the pair of amplifier inputs to the differential output of the phase detector when the input signal is restored.

30. The method of claim 23, wherein the method further includes using the output frequency of the voltage controlled oscillator for providing the feedback signal to the differential phase detector.

31. The method of claim 23, wherein the method further includes using the output frequency of the voltage controlled oscillator as an output frequency for a system clock coupled to a number of system modules connected to the communication system.